THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte DAVID R. EVOY and NICHOLAS J. RICHARDSON

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Appeal No. 1997-3156
Application No. 08/372,423

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ON BRIEF

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Before KRASS, FLEMING and LALL, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 24, 26, 28-30 and 32. Claims 16-23 have been indicated as allowable and claims 25, 27 and 31 have been canceled.

The invention is directed to monitoring the system performance of an integrated circuit in order to allow for the adjustment of operating frequency and to monitor the core temperature of the integrated circuit.

Representative independent claim 24 is reproduced as follows:

24. A system comprising:

an integrated circuit, the integrated circuit using a clock signal to generate an output signal on an output pin of the integrated circuit; and,

a monitoring circuit which monitors core temperature of the integrated circuit, the monitoring circuit comprising

a phase delay detection circuit coupled to the output pin of the integrated circuit and to the clock signal, the phase delay detection circuit including

digital signal generating means, coupled to the output pin of the integrated circuit, for generating a digital signal, wherein changes in phase delay between the output signal on the output pin of the integrated circuit and the clock signal result in changes in a duty cycle of the digital signal generated by the digital signal generating means, and

integrating means, coupled to the digital signal generating means, for integrating the digital signal to produce an integrated signal, a voltage level of the integrated signal indicating relative phase delay between the output signal on the output pin of the integrated circuit and the clock signal, and

control means coupled to the integrating means, for changing an operating frequency of the integrated circuit when the voltage level of the integrated signal indicates that the phase delay between the output signal and the clock signal is longer than a predetermined value.

The examiner relies on the following references:

Swapp	4,858,208	Aug. 15, 1989

Claims 24, 26, 28-30 and 32 stand rejected under 35 U.S.C. § 103 as unpatentable over Swapp.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

We reverse.

We have reviewed the evidence before us including, inter alia, the arguments of appellants and the examiner and we agree with appellants that the instant claimed subject matter would not have been obvious, within the meaning of 35 U.S.C. § 103, based on the evidence provided by Swapp.

Each of the independent claims requires, inter alia, the monitoring of the core temperature of an integrated circuit and a control for changing the operating frequency of the integrated circuit when a voltage level of an integrated signal indicates that a phase delay between an output signal on an output pin of the integrated circuit and a clock signal is longer than a predetermined value.

Although Swapp mentions nothing about monitoring core temperature of an integrated circuit, the examiner contends that Swapp can be used for determining temperature changes because propagation delays are known to be caused by temperature changes and Swapp measures propagation delays. Appellants argue that

it is not necessarily true that in all integrated circuits a propagation delay increases proportionally as temperature rises.

We need not reach the issue of whether temperature monitoring is suggested by Swapp because we find that Swapp clearly does not teach or suggest the claimed control for changing the operating frequency of the integrated circuit when a phase delay between an output signal and a clock signal is longer than a predetermined value.

The examiner contends that this limitation is suggested by Swapp. More particularly, the examiner urges that the skilled artisan would have recognized that comparator 34 of Swapp is meant to detect slight differences in the phases of the clock signal and the output of the device under test (DUT). The examiner concludes from this that "*if* this difference became too great the comparator *might* not compare the correct pulses, i.e., it *might* compare the clock pulse P_i with the DUT output pulse P_{i-1}" [answer-page 4, emphasis ours].

In our view, the examiner's position is based purely on speculation most likely acquired from a hindsight knowledge of appellants' invention. Swapp's disclosure is of no help in determining what would happen therein if the difference indicated by comparator 34 became "too great." It is not known at what level the comparator might not compare the proper pulses, if at all. Thus, Swapp clearly does not indicate a

"predetermined value," as claimed, of a phase delay at which the operating frequency of the integrated circuit is changed. In short, without resorting to pure speculation, there is nothing in Swapp which suggests the changing of an operating frequency of the DUT when a voltage level of an integrated signal indicates that the phase delay between the output signal of the DUT and a clock signal is longer than a predetermined value.

Accordingly, the examiner's decision rejecting claims 24, 26, 28-30 and 32 under 35 U.S.C. § 103 is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
MICHAEL R. FLEMING Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
PARSHOTAM S. LALL Administrative Patent Judge	)	

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